MICROPROCESSOR SYSTEMS

8086 Microprocessor

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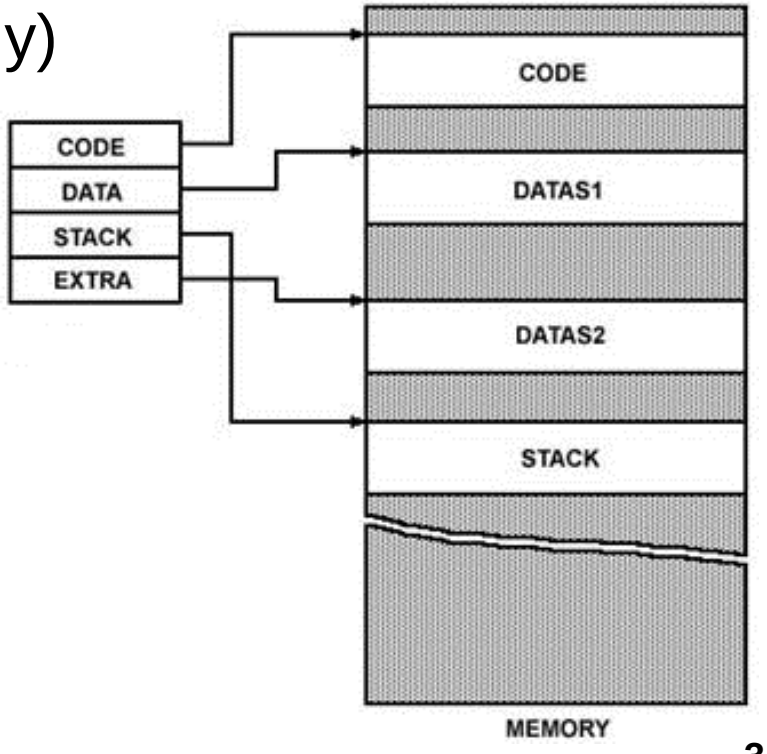
The Intel ® 8086 Microprocessor

- Intel in 1978 introduced 8086, an 16-bit microprocessor having 20-bit address line
- 40 pin DIP
- 5MHz to 10MHz clock speed
- Intel 8088 is an enhancement over 8086 having:
  - 8-bit external data bus to support
  - Allow to use few cheaper ICs to work with
- 8086 raised the x86 architecture, which is Intel's most successful line of processors.

Intel ® 8086 Microprocessor

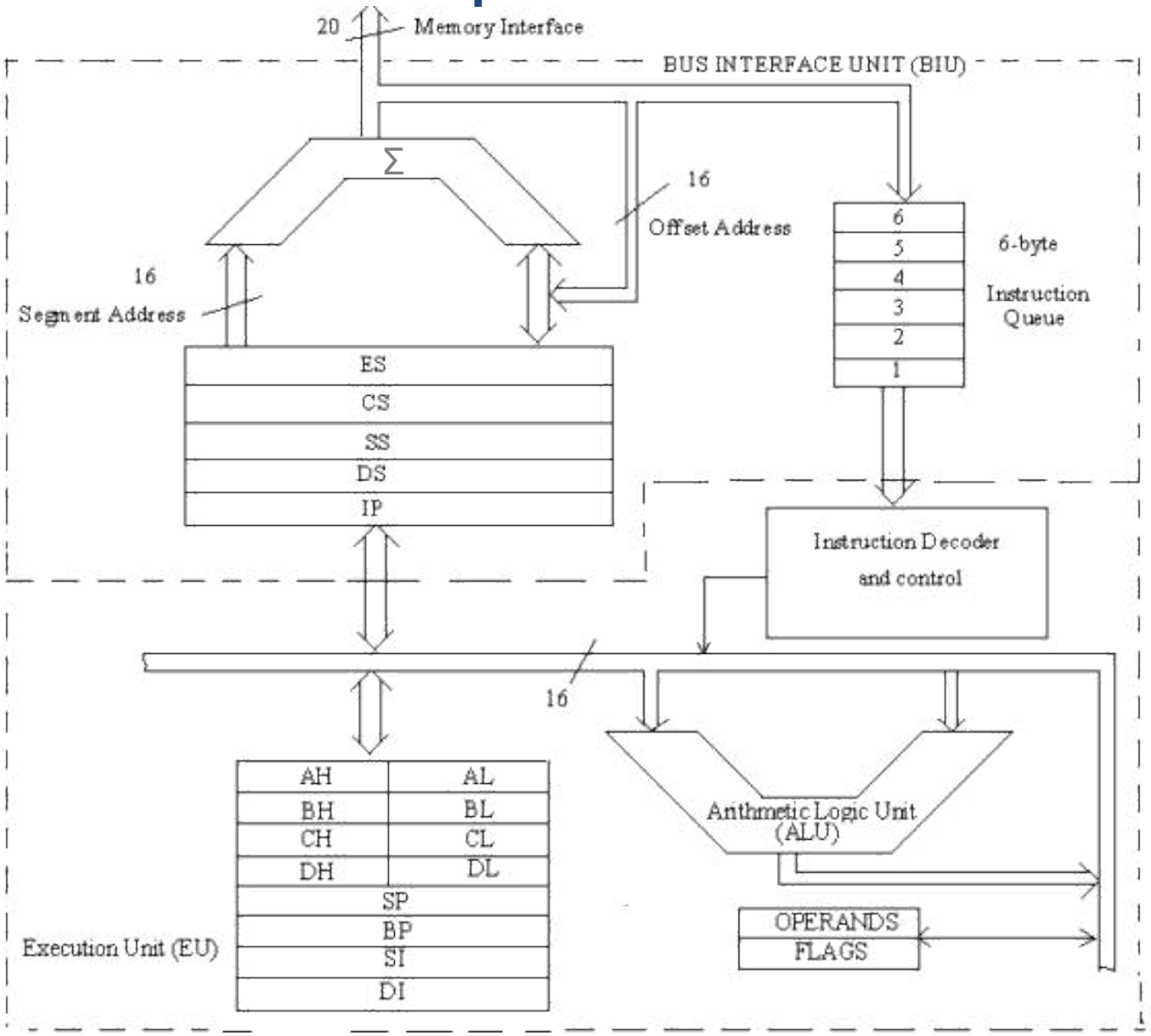
- Uses a queue to fetch instructions before these are required
  - Fetches 6 byte of instruction from memory
  - Locality of reference
  - 1 stage pipelining (fetching only)
- A program is represented in segments
  - Stack Segment
  - Code Segment
  - Data Segment
  - Extra Segment



Intel ® 8086 Microprocessor Architecture

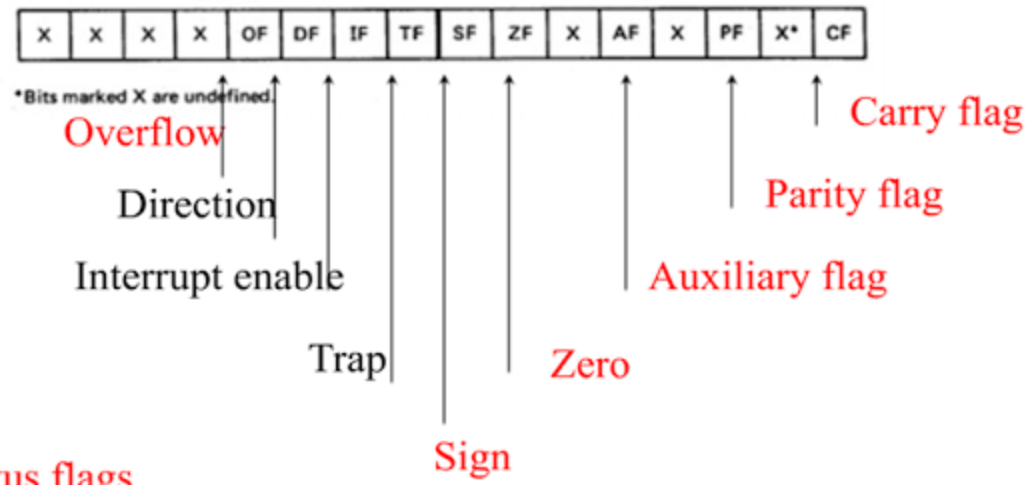
- Architecture of 8086 is divided into two logical units
- Execution Unit
  - Decodes instruction
  - Perform Execution
  - Send control signals
  - Instruct Bus Interface Unit
- Bus Interface Unit
  - Fetches Instruction with help of EU
  - Stores 6 bytes of instruction code in queue
  - Generate 20bit address using address generation unit from offset and segment address

Intel ® 8086 Microprocessor Architecture



Intel ® 8086 Microprocessor Architecture

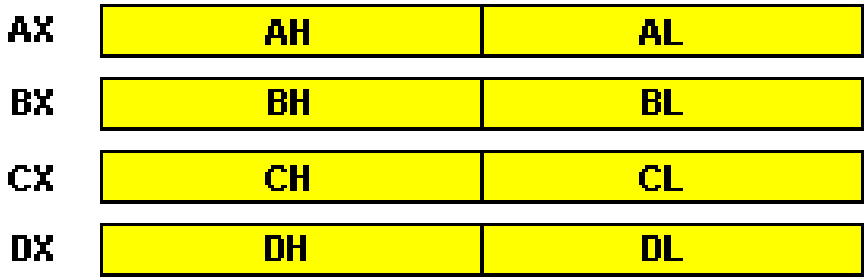
- Execution Unit contains:
  - Instruction Decoder & Control
    - Fetches instruction from instruction queue and decode it
    - Send commands to perform a task
  - ALU: Arithmetic & Logic Unit
    - Arithmetic & logic operations are executed
  - Registers
    - Flag registers
      - Status flag registers
      - Control flag registers



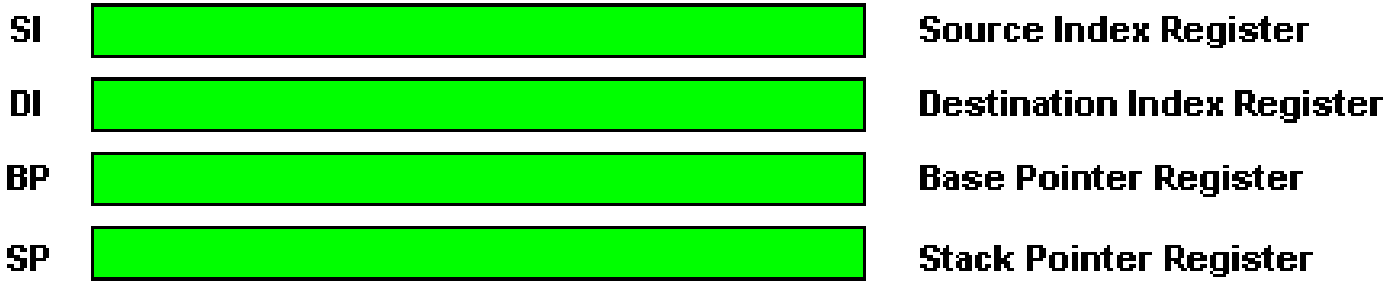
6 are status flags
3 are control flag

Intel ® 8086 Microprocessor Architecture

- Registers
  - General Purpose



  - Pointer & Indexing



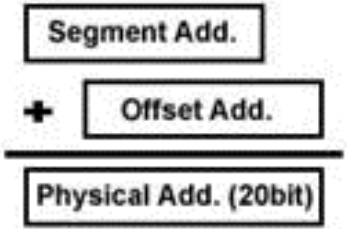
    - Base pointer and Stack pointer carries starting address of stack and address of top of the stack respectively
    - Source Index and Destination Index are usually used in string processing to identify source & destination address

Intel ® 8086 Microprocessor Architecture

- Bus Interface Unit contains:
  - Registers
    - Pointer register

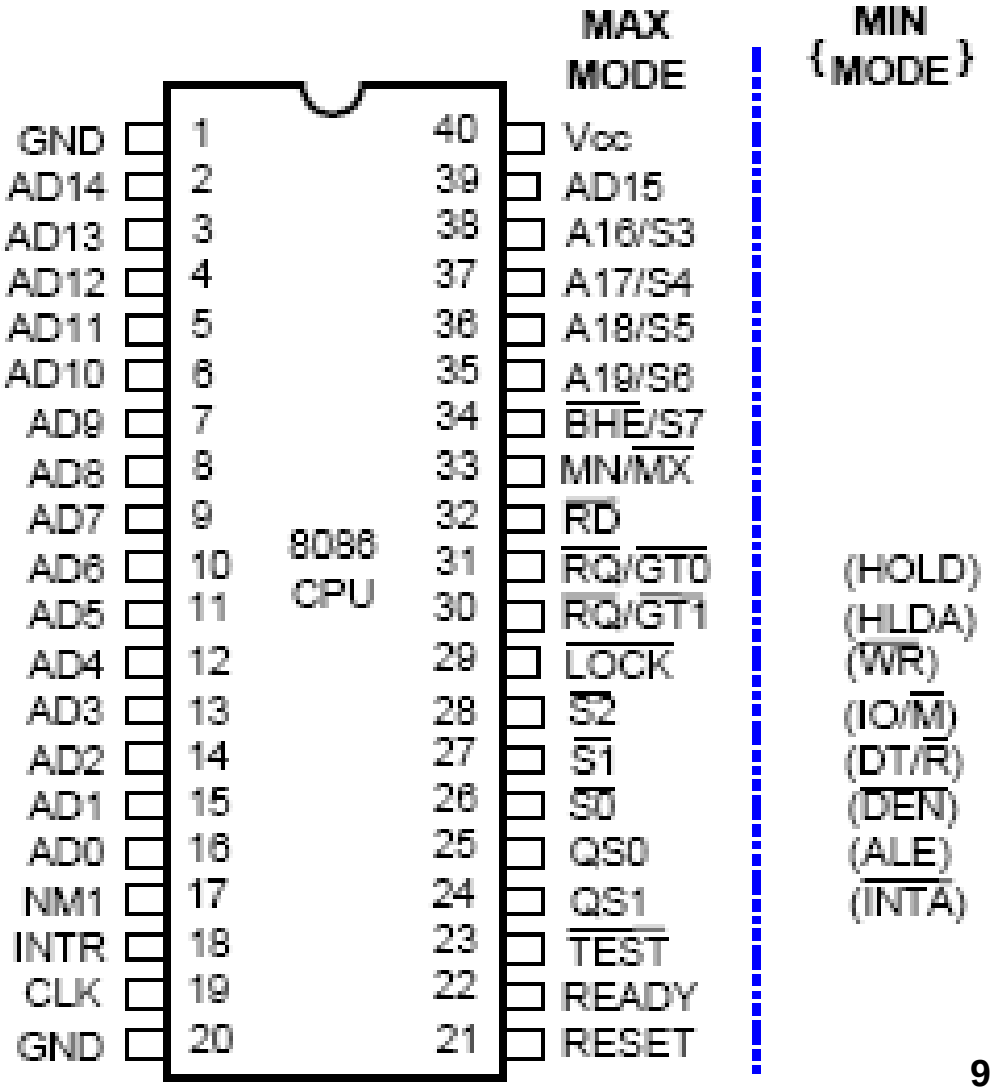
    - Segment register

  - Address Generation Unit
    - Sum-up 16-bit offset and 16-bit segment address to generate actual 20-bit physical address
    - Pads four Zero bits at MSB and four zero bits at LSB in offset and segment address respectively
  - Instruction Queue
    - Fetches 6 bytes of instructions



Intel ® 8086 Pin Configuration

- 40-pin DIP
- 8086 can work in two modes:
  - Min. Mode
    - Single processor
    - No need to use bus controller
    - Simple interfacing
  - Max. Mode
    - Multiple processor are interfaced (e.g. math-coprocessor 8087)
    - Bus controller is required (e.g. 8288 IC)
    - Master/Slave interfacing



Intel ® 8086 Pin Configuration

- µP usually have min 4 clock cycles T1, T2, T3 & T4
- Common Pins
  - Power Pins (Vcc, GND)
  - Clock Input (CLK)
  - Interrupt input, checked at last clock cycle
    - Interrupt Request (INTR)
    - TRAP/Non-maskable Interrupt (NMI)
  - Wait input (TEST) provided by delay/wait instruction
  - Ready Input (READY) from slower devices on operation completion
  - Reset Input (RESET) to restart µP
  - Read Control Signal (RD) for read operation
  - Input signal for mode selection (MN/MX)

Intel ® 8086 Pin Configuration

- Address/Data (AD0 to AD15)
  - Address is placed in T1, while data is available in remaining clock cycles
- Address/Status (A16/S3 to A19/S6)
  - Address is placed in T1, while status signal is available in remaining clock cycles
  - S3 & S4 are used to describe the segment being accessed

S4	S3	Function
0	0	Extra segment access
0	1	Stack segment access
1	0	Code segment access
1	1	Data segment access

  - S5 describes the status of Interrupt Flag
  - S6 defines control of bus over µP (HIGH) or else (LOW)

Intel ® 8086 Pin Configuration

- Byte Selection/Status (BHE/S7)
  - Bus High Enable sets the byte to transfer in T1, while status is available in remaining clock cycles
  - BHE is paired with A0

BHE	A0	Function
0	0	Whole Word
0	1	Upper byte
1	0	Lower byte
1	1	None

  - S7 defines that BHE was used, therefore is always 1

Intel ® 8086 Pin Configuration

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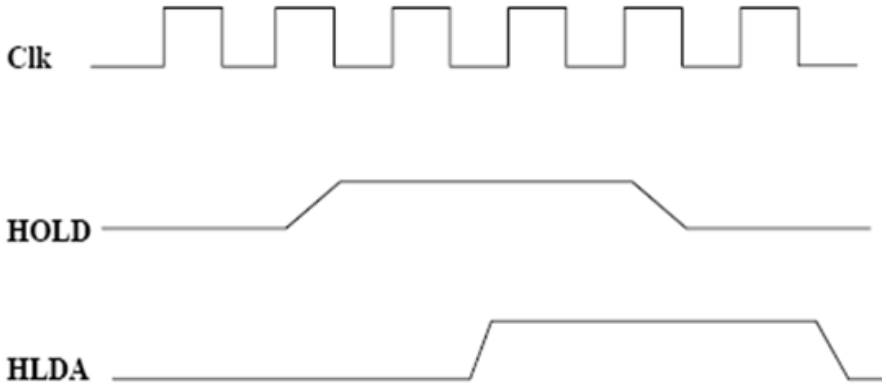
Intel ® 8086 Pin Configuration

- Minimum Mode
  - Hold the control of bus, (HOLD) is activated during current T4 and coming T1 to take control
  - Hold acknowledged (HLDA) is activated while releasing the bus



  - Write control signal (WR)
  - Input/Output or memory access signal (IO/M)
  - Transfer or receiving signal (DT/R)
  - Address Letch enable (ALE), defines address is available on AD0 to A19/S7
  - Data Enable (DEN), defines data is placed on data bus
  - Interrupt acknowledge (INTA) towards peripherals (via PIC)

Intel ® 8086 Pin Configuration

- Maximum Mode
  - Status output (S0 to S3), defines nature of operation

S2	S1	S0	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Read memory
1	1	0	Write memory
1	1	1	Passive State

  - Locked system bus (LOCK), is LOW when bus is already in use

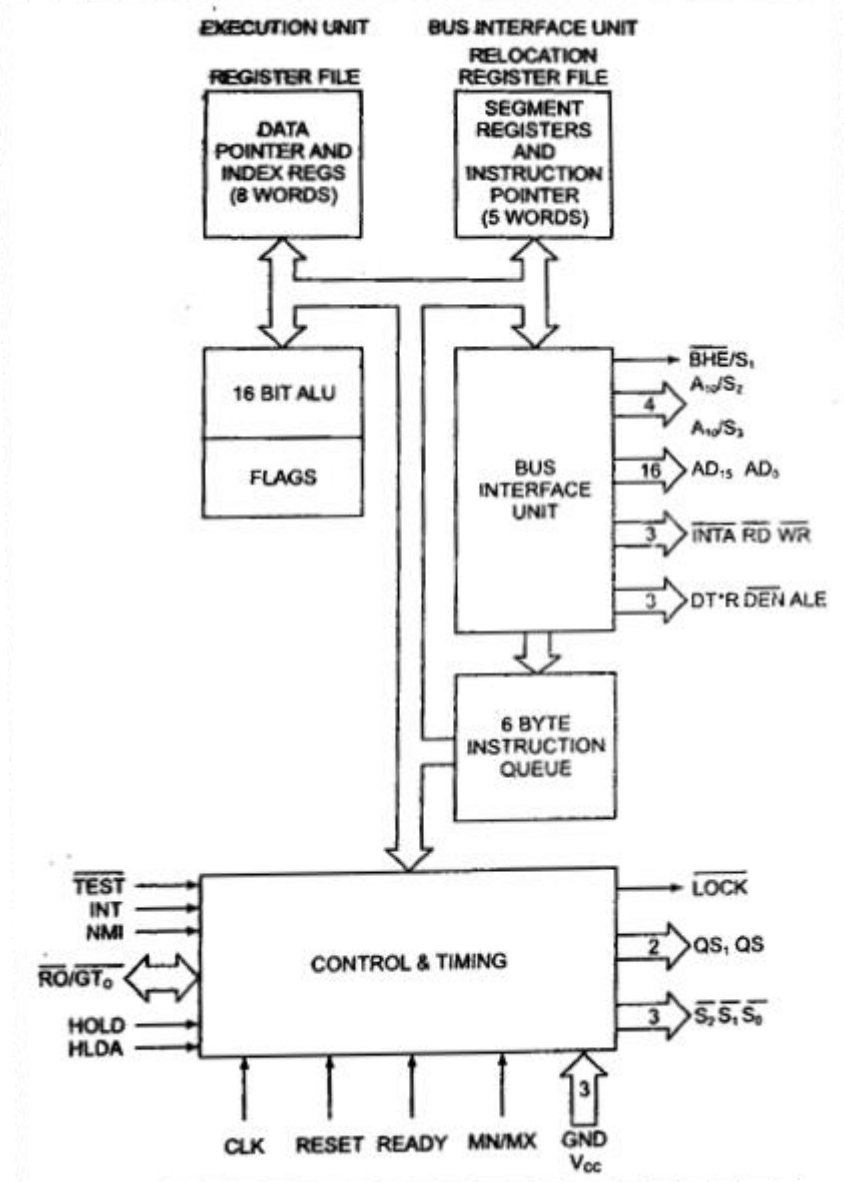
Intel ® 8086 Pin Configuration

- Maximum Mode
  - Queue Status output (QS0 & QS1), defines status of queue to external components

QS0	QS1	Characteristics
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

  - Request/Granted (RQ/GT0 & RQ/GT1)
    - This pair of pin can be used to send request and receive acknowledgement for using the bus
    - Bidirectional bus, used in multi-processor systems

The Intel ® 8086 Microprocessor



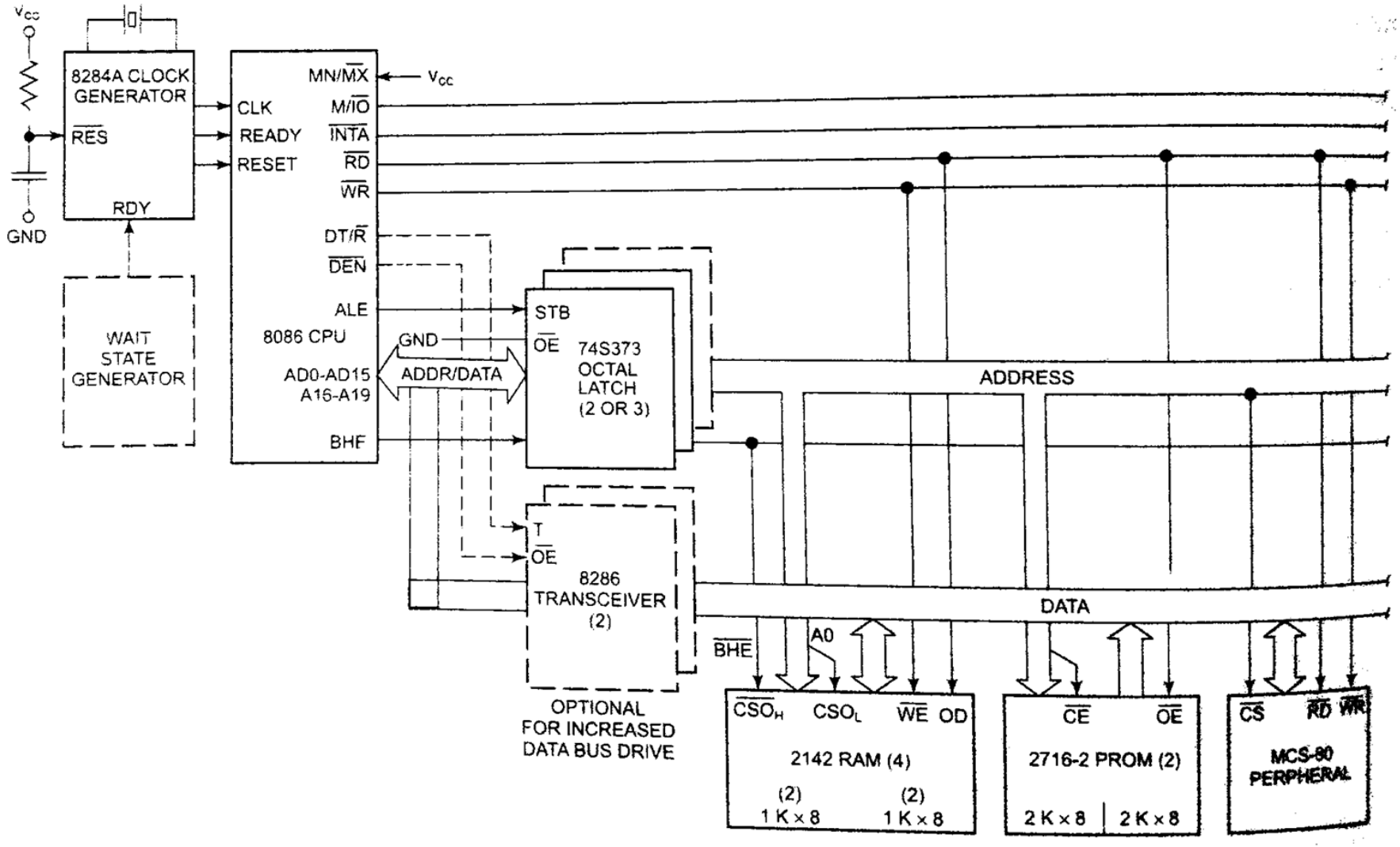
The Intel ® 8086 Microprocessor

(Min Mode)

- The simplest 8086 system can be considered in minimum mode
- 8086 processor is connected with
  - 8286 transceiver: A data buffer with capability to provide high current signal for peripheral devices.
  - 74S373 address latch: Used to hold and put the signal on bus for whole time
  - 8284 Clock generator: Clock generator is used to provide timing signals (clock, ready and reset) towards microprocessor
- All peripheral components are connected with microprocessor via system bus with help of transceiver and address latches

The Intel ® 8086 Microprocessor

(Min Mode)



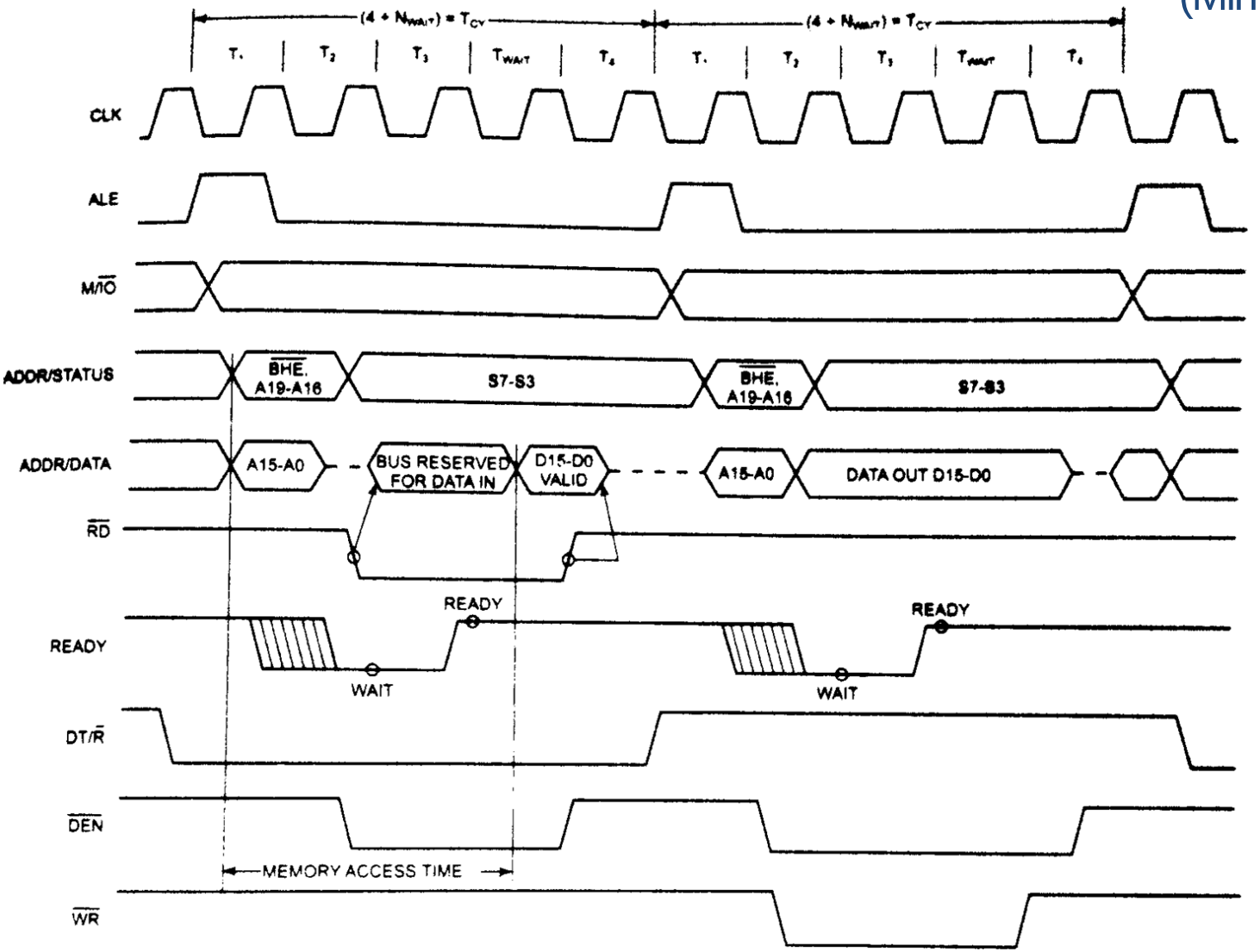
The Intel ® 8086 Microprocessor

(Min Mode)

- Working of simple 8086 processor based system can be viewed by timing diagram
- Machine cycle is combination of time cycles which are required to perform a task
  - Usually, µP requires 4 or more time cycles
- In T1, Address signals are to be generated to address particular component
- Other control and data signals are generated from T2 to T4
- An extra time cycle Tw is added for peripherals to perform R/W operations

The Intel ® 8086 Microprocessor

(Min Mode)



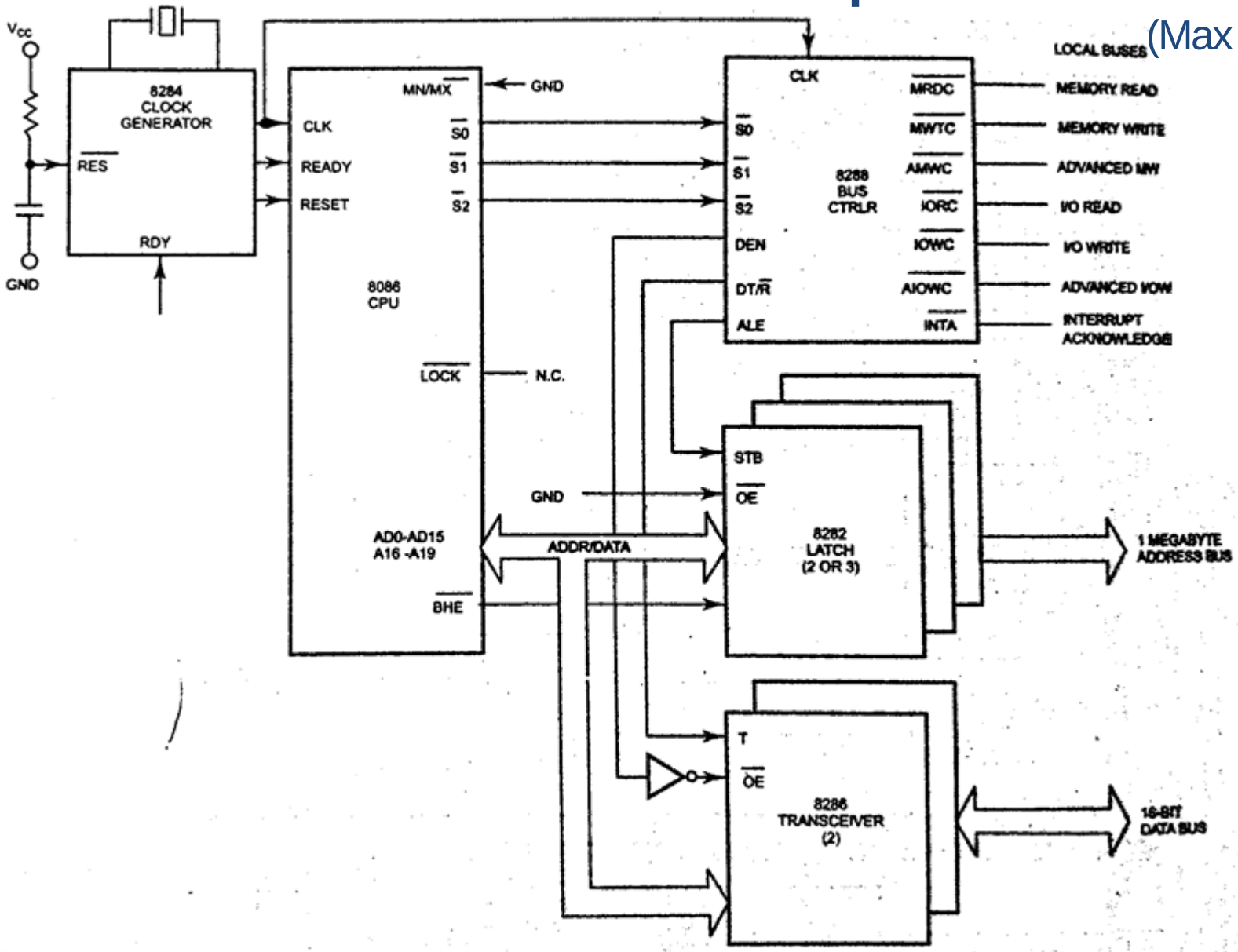
The Intel ® 8086 Microprocessor

(Max Mode)

- Maximum mode of 8086 based system requires a bus controller
- 8288 Bus controller is used to multiple controllers (e.g. µP, math-co processor etc.) to share a single system bus
- 8288 is considered as master while all other controllers are considered as slaves
- Slave sends request to master to access the system bus
- 8288 controller provide required signals to components like memory or I/O write, read etc.
- Address latches and transceivers are also connected with 8288

The Intel ® 8086 Microprocessor

(Max Mode)



Addressing modes of 8086 Microprocessor

- 8086 Microprocessor supports 8 addressing mode:
  - Direct: Offset address is present within the instruction, e.g. MOV AX, [2020H]
  - Immediate: Data operand is present within the instruction, e.g. ADD AX, 2020H
  - Register: Only Registers are involved for particular operation, e.g. ADD AX, BX
  - Register Indirect: Operation is performed between contents of Register and the contents which are pointed by another register, e.g. ADD AX, [BX]
  - Based: Offset address is added with the contents of base register, e.g. MOV DX, [BX+04]

Addressing modes of 8086 Microprocessor

- Indexed: Offset address is added with index register, e.g. MOV AX, [SI+04]
- Based-Index: Address is computed by adding index and base register, e.g. MOV AX, [BX+SI]
- Based Index with displacement: The instruction contains sum of base and index register along with displacement to compute actual address, e.g. MOV AX, [BX+SI+04]

Instruction Set Architecture of 8086 Microprocessor

- 8086 Microprocessor supports 8 types of instructions:
  - Data Transfer Instruction: Instructions involved in data transfer from source to destination.
    - Word Transfer Instruction
      - MOV – Copy contents form source to destination
      - PUSH – Push word at top of the stack
      - POP – Pop word from top of the stack
      - PUSHA – Push all registers at top of the stack
      - POPA – Pop contents of all registers from top of the stack
      - XCHG – Exchange contents b/w two locations
      - XLAT – Translate byte in AL
    - I/O port Data Transfer Instruction
      - IN – Read byte/word from provided port into accumulator
      - OUT – Write byte/word towards provided port from accumulator

Instruction Set Architecture of 8086 Microprocessor

- Address Transfer Instruction
  - LEA – Load address into provided registers
  - LDS – Load address in DS and provided register
  - LES – Load address in ES and provided register
- Flag Transfer Instruction
  - LAHF – Load flag registers into higher byte of accumulator
  - SAHF – Store contents into flag registers from higher byte of accumulator
  - PUSHF – Push flag registers' contents at top of the stack
  - POPF – Pop flag registers' contents from top of the stack

Instruction Set Architecture of 8086 Microprocessor

- Arithmetic Instruction: Instructions to perform arithmetic operations
  - Addition instructions
    - ADD - Performs addition between two operands/locations
    - ADC - Addition with carry
    - INC - Increment
    - AAA - Adjust ASCII after Addition
    - DAA - Adjust Decimal after Addition
  - Subtraction Instruction
    - SUB - Performs subtraction between two operands/locations
    - SBB - Subtraction with borrow
    - DEC - Decrement
    - NPG - Used to perform 1's & 2's complement
    - CMP - Comparison
    - AAS - Adjust ASCII after Subtraction
    - DAS - Adjust Decimal after Subtraction

Instruction Set Architecture of 8086 Microprocessor

- Multiplication instructions
  - MUL - Performs multiplication between two operands/locations
  - IMUL - Multiplication with signed operand
  - AAM - Adjust ASCII after Multiplication
- Division Instruction
  - DIV - Performs division between two operands/locations
  - IDIV - Division with signed operand
  - AAD - Adjust ASCII after Division
  - CBW - Fills byte bits into upper byte of word
  - CWD - Fills word bits into double word

Instruction Set Architecture of 8086 Microprocessor

- Bit Manipulation Instruction: Instructions to manipulate bit or set of bits
  - Logical operation Instruction
    - AND – Adding each bit with corresponding bit of byte/word
    - OR – Multiplying each bit with corresponding bit of byte/word
    - XOR – Exclusive OR over each bit with corresponding bit of byte/word
    - NOT – Inverting each bit with corresponding bit of byte/word
    - TEST – Update flags by adding operands but without affecting their data
  - Shift operation Instruction
    - SHL – Shift bits towards left and add zeros at LSB
    - SHR – Shift bits towards right and add zeros at MSB
    - SAL – Shift bits towards left and copy old LSB to new LSB
    - SAR – Shift bits towards right and copy old MSB to new MSB

Instruction Set Architecture of 8086 Microprocessor

- Rotate operation Instruction
  - ROL – Rotate bits towards left by moving MSB to LSB and to CF
  - ROR – Rotate bits towards left by moving LSB to MSB and to CF
  - RCR – Rotate bits towards right with carry by moving LSB to CF and CF to MSB
  - RCL – Rotate bits towards left with carry by moving MSB to CF and CF to LSB

Instruction Set Architecture of 8086 Microprocessor

- String Instruction: Instructions involved in string manipulation
  - REP – Repeat instruction until CX ≠ 0
  - REPE – Repeat instruction until CX = 0
  - RPEZ – Repeat instruction until ZF = 0
  - REPNE – Repeat instruction until CX ≠ 0
  - REPNZ – Repeat instruction until ZF ≠ 0
  - MOVS – Move string b/w source and destination
  - MOVSB– Move string byte
  - MOVSW– Move string word
  - COMPS – Compare two string
  - COMPSB– Compare two string bytes
  - COMPSW– Compare two string words
  - INS – Input string from port to provided memory location
  - INSB – Input string byte from port to provided memory location
  - INSW – Input string word from port to provided memory location

Instruction Set Architecture of 8086 Microprocessor

- OUTS – Output string from provided memory location to port
- OUTSB – Output string byte from provided memory location to port
- OUTSW – Output string word from provided memory location to port
- SCAS – Scan and compare string with the contents of accumulator
- SCASB – Scan and compare string byte with the contents of AL
- SCASW– Scan and compare string word with the contents of AX
- LODS – Load string into accumulator
- LODSB– Load string byte into AL
- LODSW– Load string word into AX

Instruction Set Architecture of 8086 Microprocessor

- Execution Transfer Instruction: Instructions involved in altering the sequence of execution
  - Without condition
    - CALL – Call a procedure and save the returning address into the stack
    - RET – Return from calling function
    - JMP – Jump from one instruction to another
  - With conditions
    - JA - Jump if above
    - JAE - Jump if above or equal to
    - JNB - Jump of not below
    - JNBE - Jump if not below or equal to
    - JC - Jump of CF = 1
    - JE - Jump if Equal
    - JZ - Jump if ZF = 1
    - JG - Jump if greater than
    - JNLE - Jump if not less than or equal to

Instruction Set Architecture of 8086 Microprocessor

- JGE - Jump if greater than or equal to
- JNGE - Jump if not greater than or equal to
- JL - Jump if less than
- JNL - Jump if not less than
- JLE - Jump of less than or equal to
- JNG - Jump if not greater than
- JNC - Jump of CF = 0
- JNE - Jump of not equal
- JNZ - Jump of ZF = 0
- JNO - Jump if OF = 0
- JNS - Jump if SF = 0
- JO - Jump if OF = 1
- JP - Jump if PF = 1
- JPE - Jump if even parity PF = 0
- JS - Jump if SF = 1

Instruction Set Architecture of 8086 Microprocessor

- Processor Control Instruction: Instructions involved in controlling processor flag registers
  - STC – Set CF = 1
  - CLC – Clear CF
  - CMC – Complement CF
  - STD – Set DF =1
  - CLD – Clear DF
  - STI – Set IE = 1 (interrupt enable)
  - CLI – Clear IE (disable interrupt)
- Iteration Control Instruction: Instructions to repeat particular piece of instructions
  - LOOP – Loop group of instructions until CX = 0
  - LOOPE – Loop group of instructions until CX = 0
  - LOOPZ – Loop group of instructions until ZF = 0
  - LOOPNE – Loop group of instructions until CX ≠ 0
  - LOOPNZ – Loop group of instructions until ZF ≠ 0
  - JCXZ – Jump to provided address if CX = 0

Instruction Set Architecture of 8086 Microprocessor

- Interrupt Instruction: Instructions involved in interrupting program execution
  - INT - Interrupt program and call specific service
  - INTO - Interrupt program and call service if OF=1
  - IRET - Return from interrupt service to calling program

Questions