MICROPROCESSOR SYSTEMS

8085 Microprocessor Interfacing

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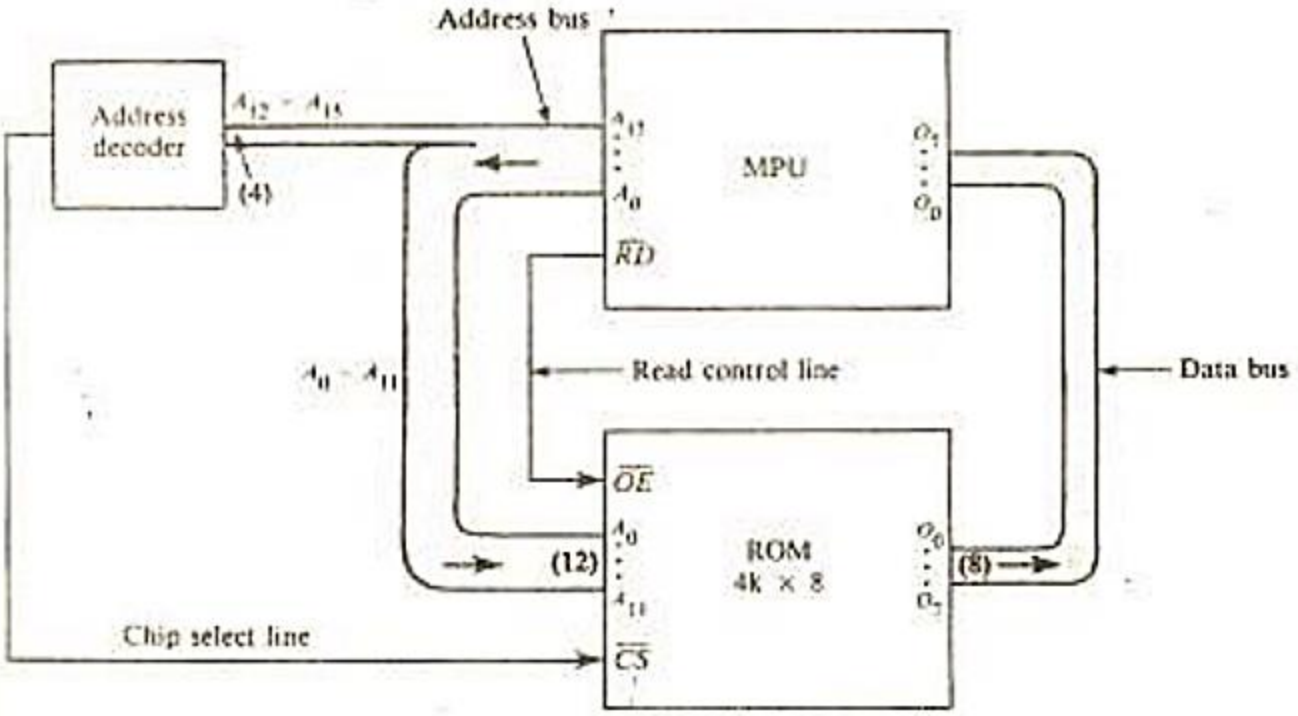
Interfacing concepts

- It is defined as:
  - “The interconnection, or linkage of the parts with in the system is called interfacing”
- Without the peripheral devices, a microprocessor is not of much use
- The interfacing is the way to get the microprocessor communicated with the peripherals
- Address, data and control bus play an important role in interfacing
- Usually MPU is the focus of all the operations unless the DMA
- I/O controllers / ports
- Programmable ports

Interfacing of microprocessor with ROM

- The system has 16 address lines and 8 data lines
- Data lines are unidirectional and connected directly with the outputs of ROM



Interfacing of microprocessor with ROM (Contd.)

- 12 Address lines are for selecting a byte in a ROM IC while 4 lines are to select an IC module
- RD* line is a control signal used to enable module
- 12 lines can access any one of 4096 locations
- The address decoder can select any one of 16 modules
- For example if A0-A11=000h and A12-A15=0h then MPU wants to access first byte of the module 0000_2

Interfacing of microprocessor with ROM (Contd.)

- A total of 16 X 4K segments can be formed
- Address decoder makes it sure that only one segment is active at a time
- Four Most significant bits of the address selects the segment

  Segment 0 → 0000h – 0FFFh

  Segment 1 → 1000 – 1FFFh

  .

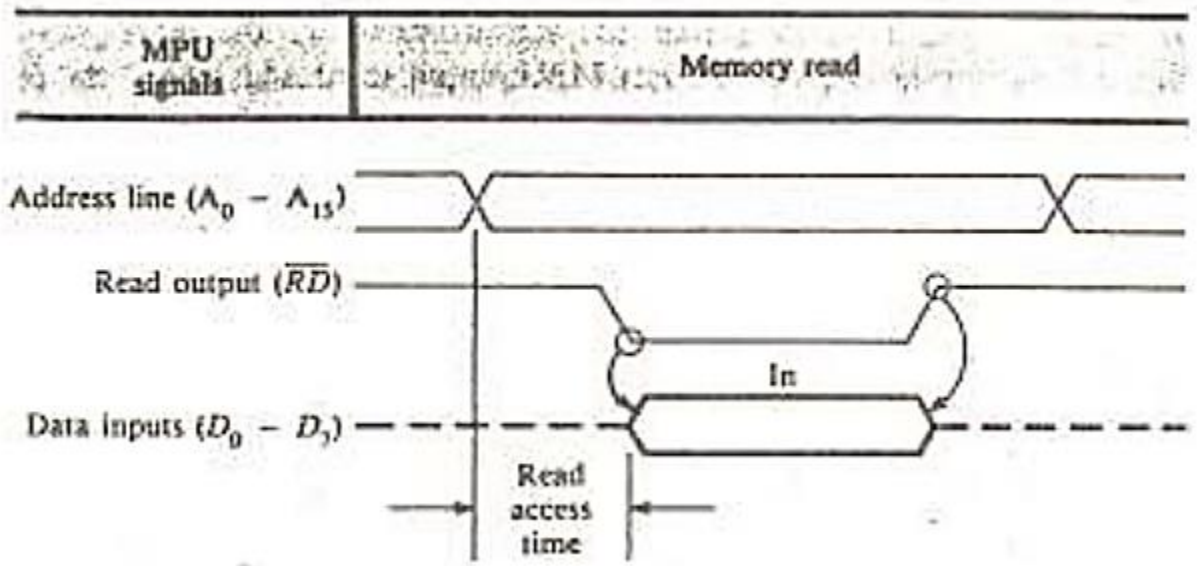
  .

  .

  Segment 15 → F000h – FFFFh

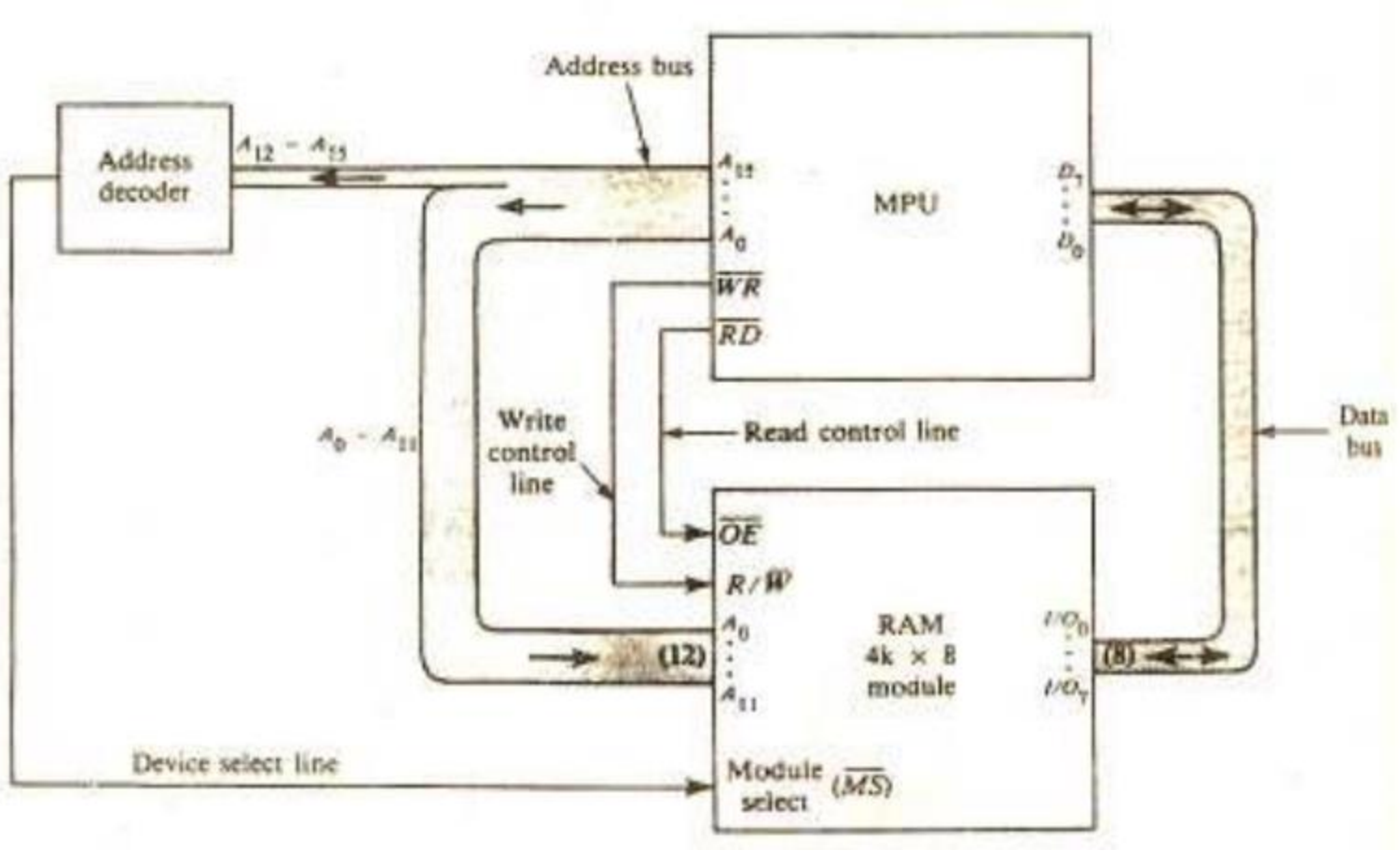
Timing Diagram

- Read Access Time is the time taken by the memory to locate the byte in the module
- H-to-L transition causes data bus to switch from tri-state to accept data
- The dashed line show the tri-state
- L-to-H transition causes the data to go back to Tri-state condition



Interfacing with RAM

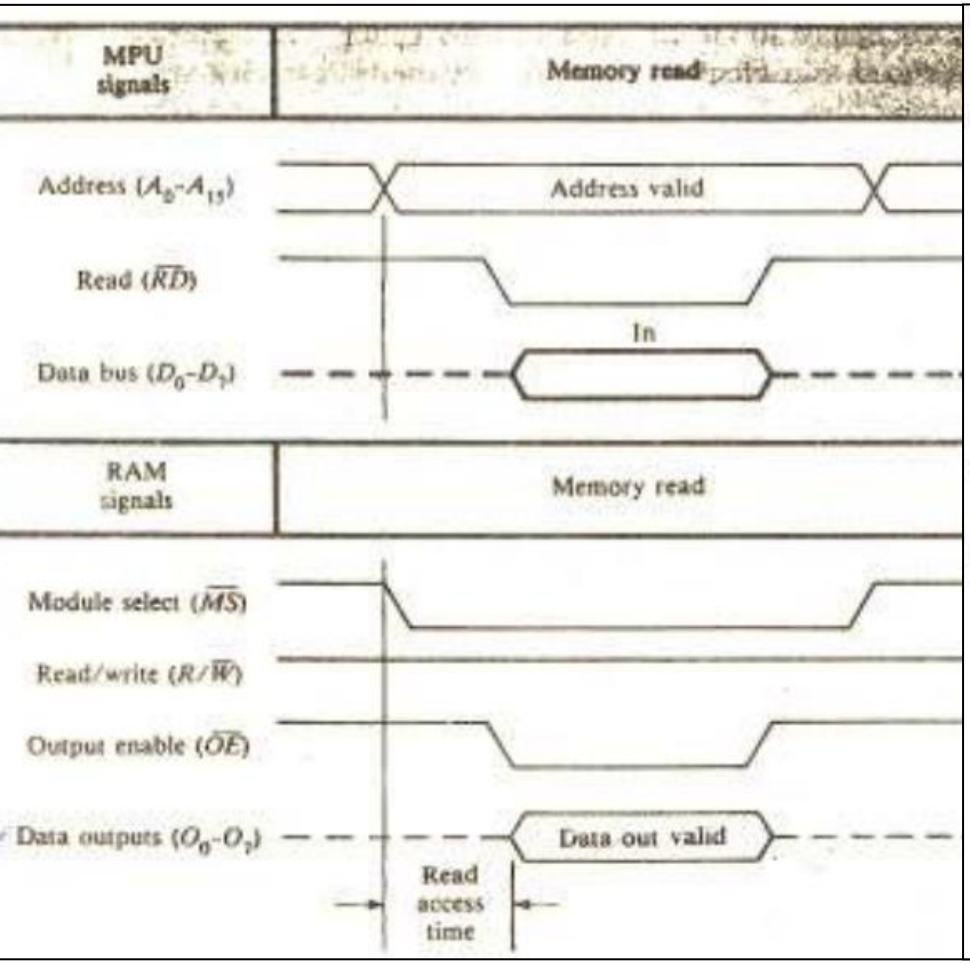
- A 4K X 8 bits RAM is shown

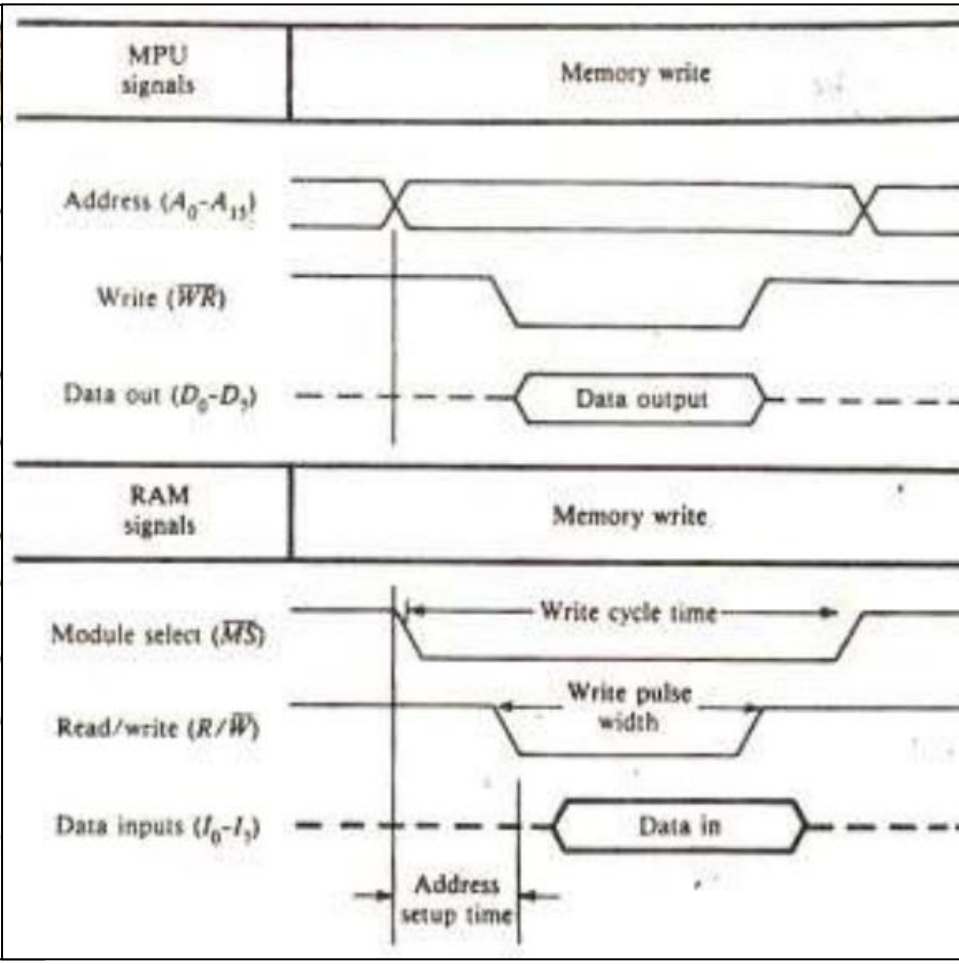


Interfacing with RAM (Contd.)

- Segment 2 is shown as 4K Byte RAM
- Address Decoder will select one of the module using 4 Most Significant Bits of the address
- Data bus is now a 2-way path and one more control signal is added (R/W*)

Interfacing with RAM (Contd.)



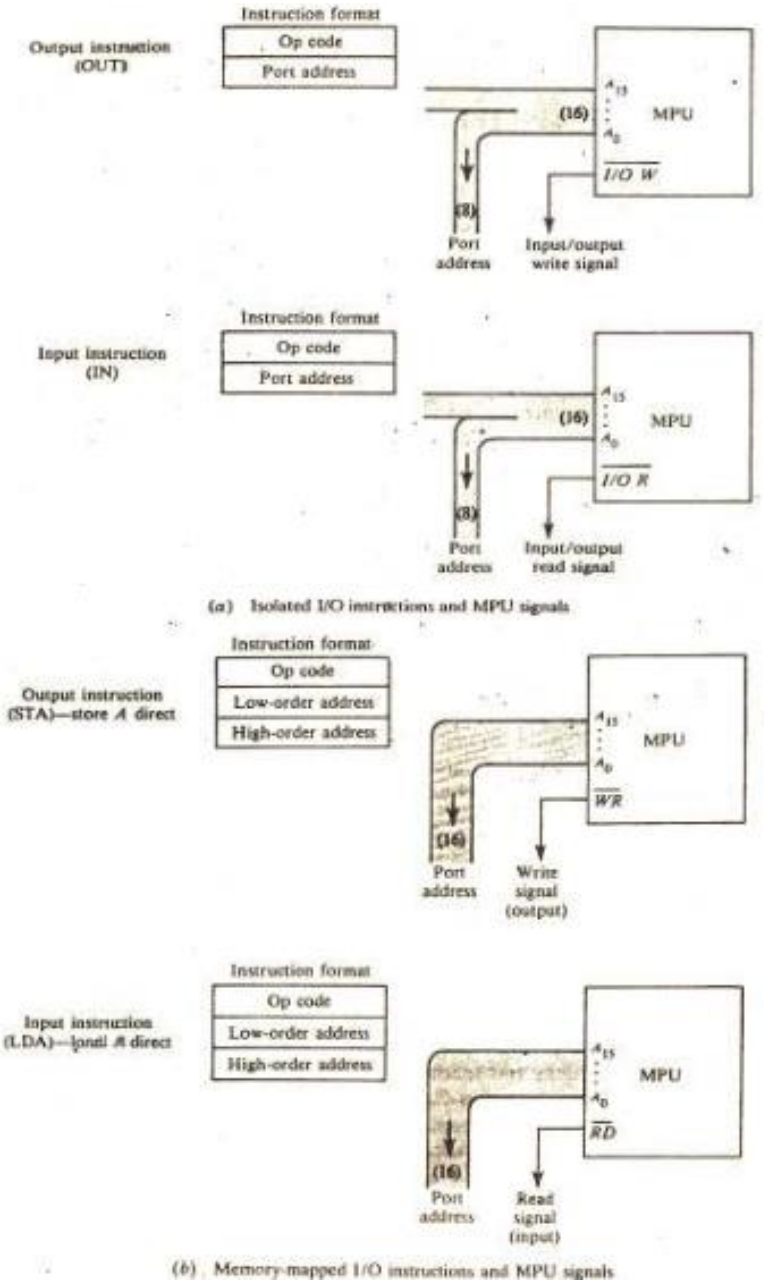


I/O Interfacing

- Input and output ports are locations where the data is stored/buffered for the device
- Generic microprocessor has IN and OUT instructions for reading and writing the port data
- If there are byte long port addresses then a system can have a maximum of 256 ports
- The port addresses come on Least Significant 8 bits of the address bus (A0-A7)
- Special (I/O W)* and (I/O R)* signals for OUT in IN instruction
- This sort of I/O is called “Isolated I/O”
- Usually the I/O data transfers are initiated by an Interrupt
  - Interrupt Service Routine (ISR)

I/O Interfacing

- There can be two types of Programmed I/O techniques
  - **Isolated I/O**: The data transfer using IN and OUT instructions where ports are addressed using a separate memory space
  - **Memory-mapped I/O**: The ports are addressed like regular memory locations and the memory-CPU data transfer instructions can be used to transfer data to and from the ports



I/O Interfacing (Contd.)

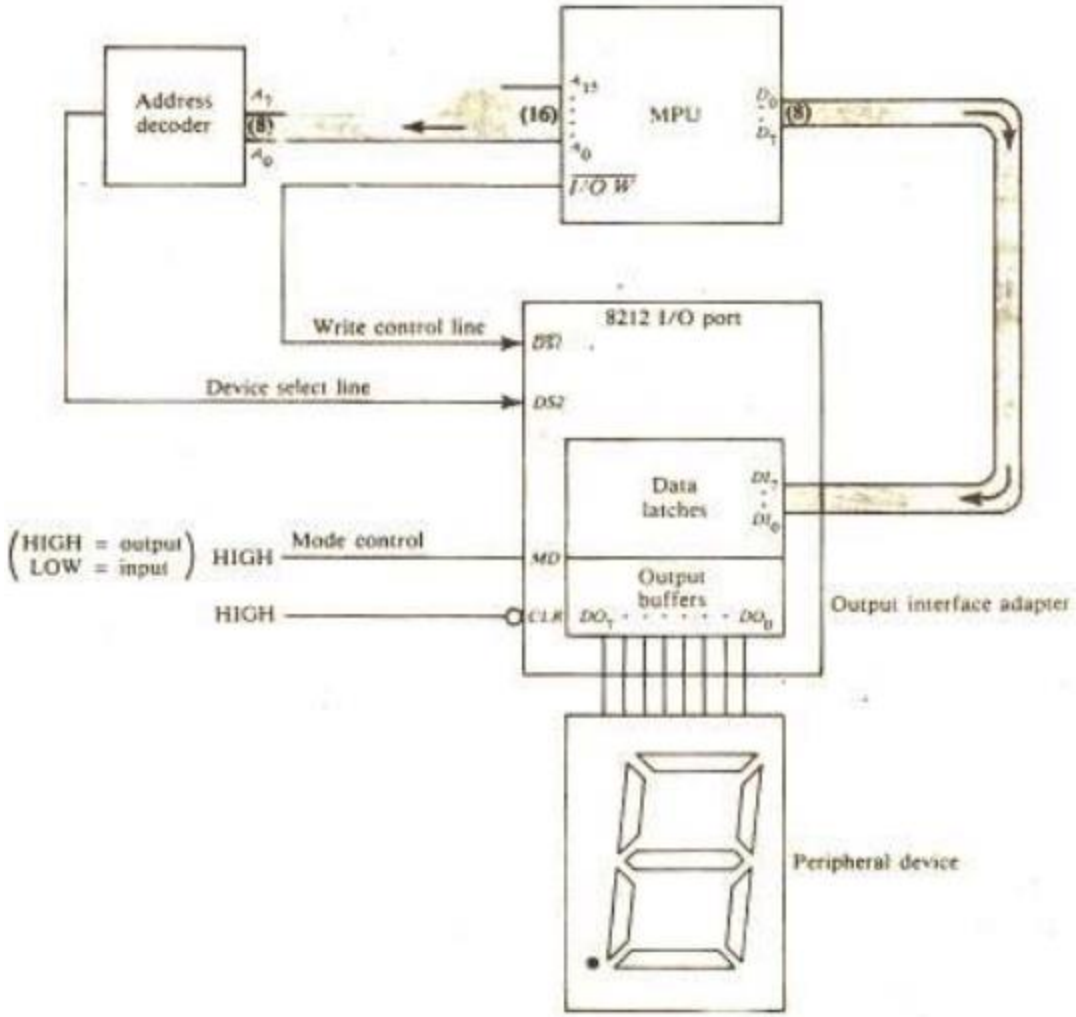
- The memory-mapped I/O is most common in microprocessors since Isolated I/O requires special instructions to do I/O
- Usually the peripheral devices are not directly connected to the MPU
- An input / output interface adapter facilitates the communications through communication and buffering

I/O Data Synchronizing

- Data transfer from I/O needs synchronizing due to the speed difference of MPU and the peripheral devices (like keyboard)
- Synchronizing is important because it is not necessary that when ever MPU refers to the ports there is a valid data
- I/O Data Transfer techniques include:
  - **Polling**: Where the CPU after executing each instruction / number of instructions looks for the valid data on the ports
  - **Interrupts**: Where some control signals are used to inform CPU / device about the valid data
- If the System is using the polling method, CPU would continuously repeat the read-output-read-output sequence
- The polling would take longer CPU times if the I/O devices are more

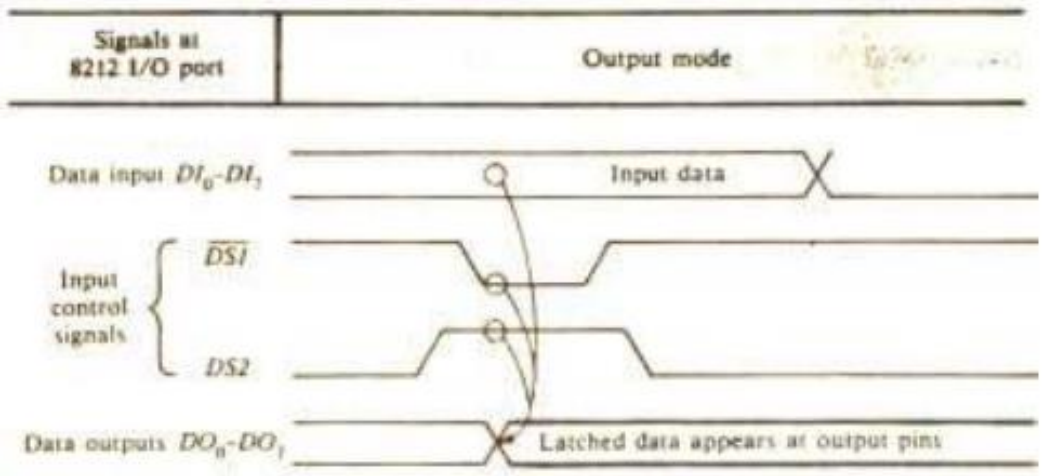
Intel® 8212 I/O Port

- Its an 8-bit input/output port IC
- A Seven Segment display is interfaced using Intel 8212 I/O port
- The system uses Isolated technique for I/O since lower 8-bits can fully decode the port



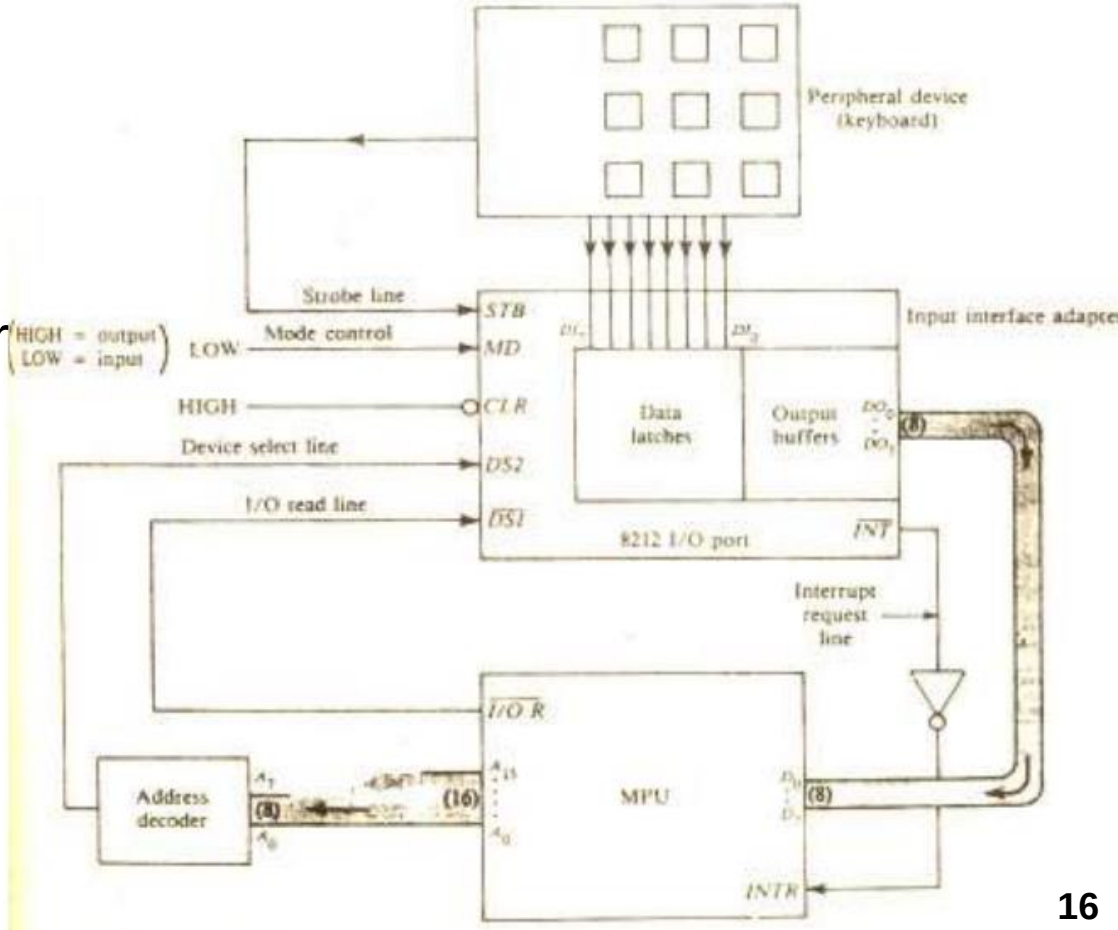
Intel® 8212 I/O Port

- The port is being used as an output port in this case because the *"Mode Control"* lines is High
- Internally the port have internal latches and buffers
- 2 "*Device Select* " lines control the flow of data to and from CPU
- When DS1* is LOW and DS2 is high, the device is ready to send / receive data



Intel® 8212 I/O Port

- The system uses interrupt based system to synchronize the input / output
- An MPU is interfaced with a keyboard input device using Intel 8212 I/O port
- The INTR line of a generic microprocessor when goes high, the MPU suspends the current task and executes ISR

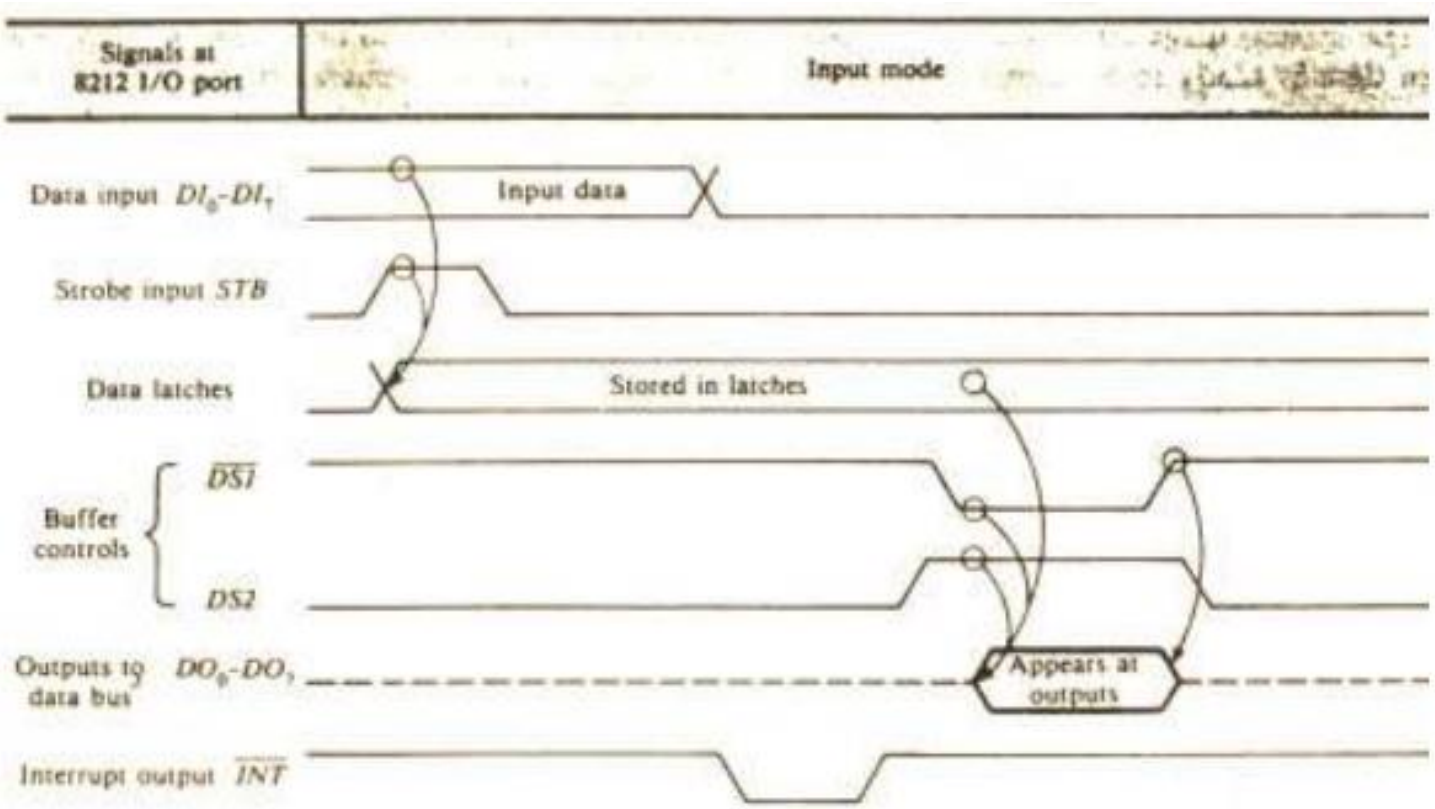


Intel® 8212 I/O Port

- After performing ISR, the MPU will return to the suspended task
- The ISR may be as simple as reading and storing a key code from keyboard device
- The 8212 port is configured as input mode since MD (Mode Control) line is low while the CLR input is disabled via a HIGH on CLR
- The 8-bit from the peripheral arrives at Data latches through input buffers (DI0-DI7)
- The peripheral uses STB line to control / latch the data in the input buffers
- The output buffers are enabled by the DS1* and DS2 line by the CPU

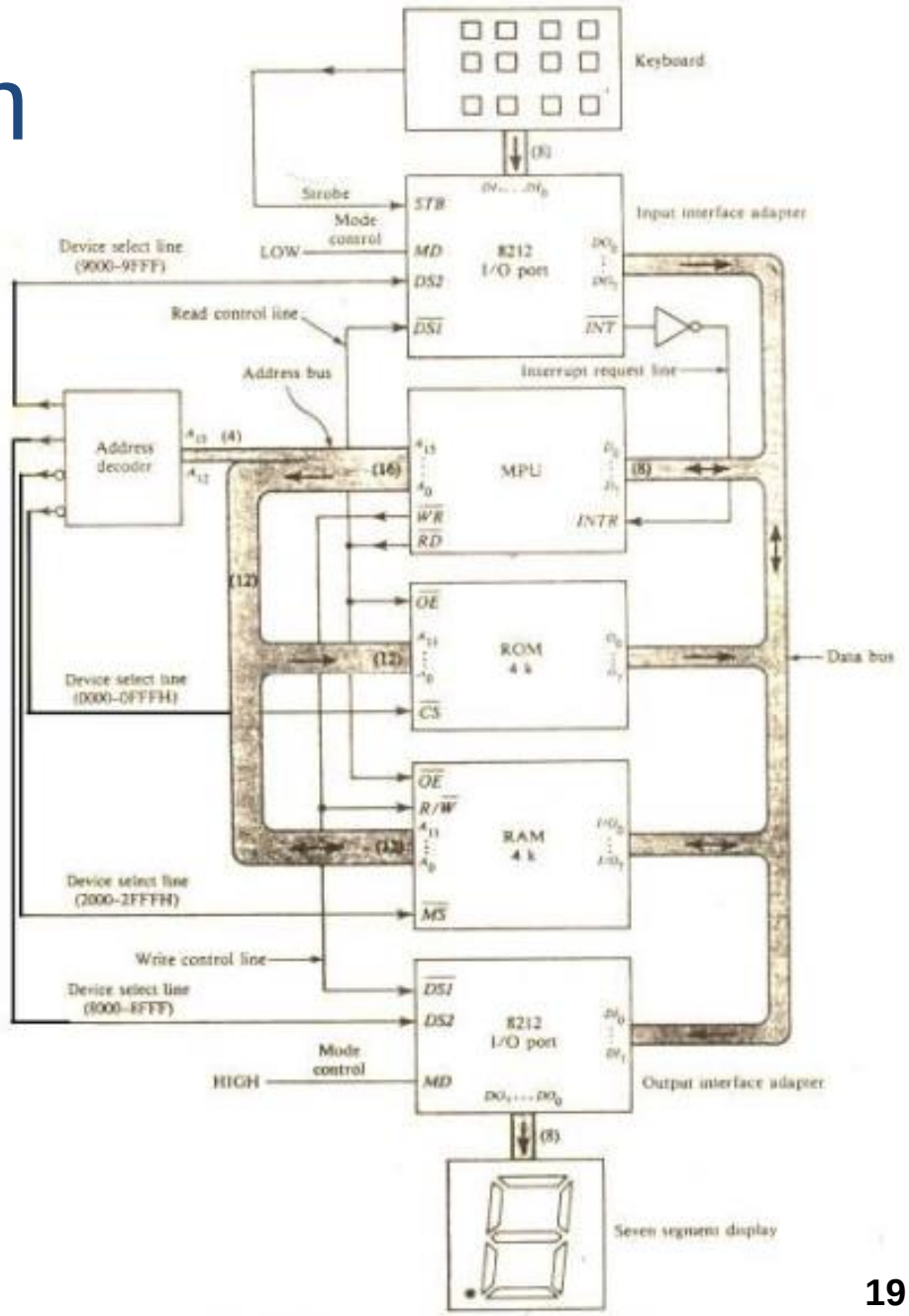
Intel® 8212 I/O Port

- 8212 informs the CPU about the data using INTR line of MPU
- CPU then activates the buffers through DS1* and DS2 lines
- The data is then output on the data lines



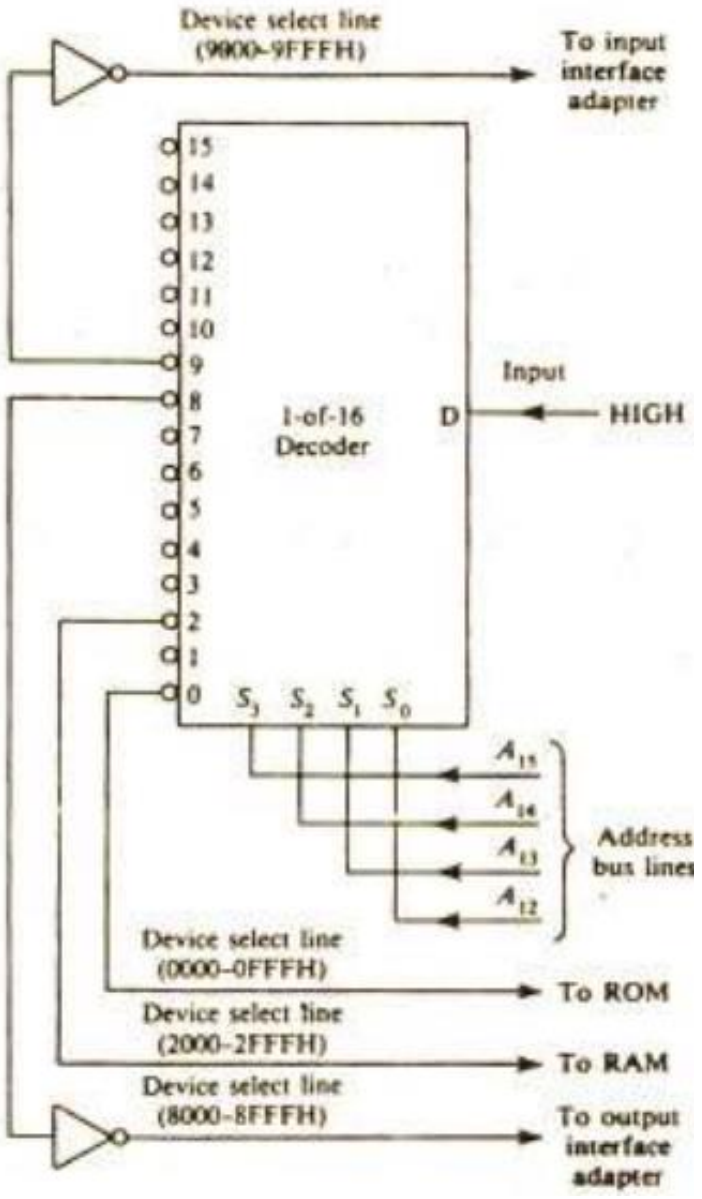
8085 based system

- A simple digital computer system that input data through keypad and output is shown through seven segment display
- The input and output operations are supported by 8212 I/O port



Address Decoding

- The system uses memory mapped input / output because the lower 8-bits of the address bus are decoded to select any one of the I/O ports



Questions